



IEEE Electrical Design of Advanced Packaging and Systems

16th December – 18th December, 2018

CHANDIGARH, INDIA

Call for Papers

The IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium is the premier international conference in Asia-Pacific region to share the recent progress of design, modeling, simulation and measurement related to the electrical issues arising at the chip, package and system levels. Covering the paper presentations, industry exhibitions, workshops and tutorials, the EDAPS 2018 will be held at the **Taj Chandigarh, in Chandigarh, India from December 16 to 18, 2018**. The technical program of the symposium not only addresses the current technical issues but also brings out the topics on IC design, SiP/SoP packaging, EMI/EMC, EDA tools and most importantly the challenging issues in advanced 3D-IC and TSV design. For further information, please consult the web site at www.edaps2018.org.

IMPORTANT DATES

Paper Submission Portal Open: **July 15, 2018**

Paper Submission Closed: ~~August 21, 2018~~ **September 10, 2018**

Acceptance Notification: **September 30, 2018**

www.edaps2018.org



TOPICS

- 3D-ICs/TSVs/Interposers
- Testing on 3D-IC and SiP
- Signal and Thermal Integrity
- Power Integrity/Power Distribution Networks (PDNs) /Ground Noise
- Computational Electromagnetics and Multi-physics Methods for SI/PI/TI Analysis
- Thermal Management Design for 3D-ICs and SiP
- Design and Modeling for High-speed Channels and Interconnects
- High speed serial links jitter budgeting
- Jitter segregation algorithms and tools
- Time / Frequency Domain Measurement Techniques
- Power supply induced jitter and transfer functions.
- Nanoelectronics for 3D-ICs and SiP

- Machine Learning applied to packaging
- Active Devices and Circuit Modeling Technologies
- Electronic Packages, SiP/ SoP
- IC and Package Level EMC
- Antennas in Packages (AiP)
- RF/mm-wave and THz Packages
- Miniaturized and Embedded Passives
- Power Electronic Packages
- Advanced Simulation Tools and CAD
- Substrate Technology for Packages and PCBs
- Electrical Design of Flexible Devices and Sensing
- 2-D Materials for 3D-ICs and SiP
- 3-D ICs and SiP Reliability
- Electrical Design for 5G Wireless Communication
- DDR's Signal and Power integrity considerations
- Others

STUDENT TRAVEL GRANTS - A limited number of travel grants will be provided to support students of accepted papers. Selection will be based on papers submitted and requires paper presentation by the student at the conference.

PAPER SUBMISSION

All papers should be submitted electronically in **two-column and three-page** PDF file format. All submissions must be made through EDAPS website (www.edaps2018.org). A Microsoft Word template is available on the symposium website. Hardcopy submission will NOT be accepted. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Non-compliant manuscripts will not be considered for review. An IEEE copyright transfer form completed with paper title, author(s) name(s) and authors' signatures should be submitted at the time of the paper submission. Files with scanned signatures are considered valid documents. Please check back with the symposium website (www.edaps2018.org) for updates on the paper submission. **Selected papers will be invited for publication in the IEEE Transactions on Components, Packaging and Manufacturing Technology.**